**Sirius 4-lane MIPITX design Spec**

1. Feature:

Support up to 4-lane 1.5Gbps, lane number can be configured as 1/2/3/4

Support up to 4K @30fps video.

Support RGB888/YUV422 8bit. 10bit / YUV420 8bit.10bit / YUV420 8bit legacy mode.

1. Top diagram



1. Clock used:

ix\_clk clock, configured by PIXEL PLL,

hs\_clk0, generated by TXPLL0

hs\_clk1, generated by TXPLL1

1. Buffer used:

From pixel to hs\_clk0 domain, 512x48 SRAM used.

TX\_CTRL interface with DPHY: 16x8 register used.

1. Free running pattern gen for test purpose.
2. Registers